REMARKS

Claims 1-7 are pending in the present application. Applicants respectfully request reconsideration of the present application in view of the remarks presented herein.

Classification

The Examiner alleges Group I, recited in Claims 1-7, as classified in class 717, subclass 131. This class is defined as "data processing: software development, installation, and management, software program development tool [e.g., integrated case tool or stand-alone development tool], testing or debugging including analysis of program execution."

Applicants assert that embodiments in accordance with the present invention as recited in Claims 1-7 are not directed to software development, software installation and/or management or software program development tools, as set forth in class 717, subclass 131. Rather, Claims 1-7 are directed to "a method of executing a processor instruction."

The differences are fundamental. For example, a software development tool, e.g., a complier, may create a sequence of computer instructions. In

contrast, Claims 1-7 are directed to a method of executing a processor instruction, e.g., of such a sequence created by a software development tool. The methods of Claims 1-7 do not create software as set forth in 717/131, but rather execute software.

For this reason, Applicants respectfully request the Examiner to classify the present application in a more applicable classification.

Restriction

It is well established that piecemeal examination should be avoided as much as possible. MPEP 707.07(g). In addition, all restriction/election requirements should normally be made before any action on the merits. 37 CFR 1.142(a) and MPEP 811. In the present application, there were at least two actions on the merits prior to the restriction requirement. The Applicants also respectfully assert that no amendments to the claims necessitated the current restriction/election requirement as the alleged limitations that render the groups separate and distinct were present in Claims 1-45 as originally presented.

As the restriction requirement is untimely, e.g., was presented after at least two actions on the merits, Applicants respectfully request withdrawal of this requirement.

MPEP § 803 explains that restriction is only proper if "[t]here would be a serious burden on the examiner if restriction is not required (see MPEP § 803.02, § 808, and § 808.02)." Applicants note that all recited claims were previously examined, in rejections dated 6/26/06 and 12/20/06. Such history of previous examination appears to infer that the examination is not seriously burdensome, and that therefore the required "serious burden" is not present.

For this reason, Applicants respectfully assert that the present six-way restriction requirement is improper, and respectfully solicit withdrawal of the restriction requirement.

"If the search and examination of all the claims in an application can be made without serious burden, the examiner must examine them on the merits, even though they include claims to independent or distinct inventions" (MPEP § 803, emphasis added).

As the previous examination has established that examination of all claims of the present application is not a "serious burden," Applicants

respectfully assert that the MPEP directs the Examiner to examine all claims of the present application on the merits. For this additional reason, Applicants respectfully assert that the present restriction requirement is improper, and respectfully solicit withdrawal of the restriction requirement.

Moreover, the previous rejections dated 6/26/06 and 12/20/06 contained at least one single rejection against claims from all of the newly alleged independent inventions. For example, Claims 1-5 (newly alleged Group I), 8, 9-14 (newly alleged Group II), 17, 18, 20 (newly alleged Group III), 23 (newly alleged Group IV) and 34-36 (newly alleged Group V) and 37 (newly alleged Group VI) were rejected under 35 U.S.C. § 102(b) as being allegedly anticipated by Nunomura (US 6,871,274, "Nunomura").

Applicants respectfully assert that the previous rejection of claims representing all of the newly alleged inventions over a single piece of art under 35 U.S.C. § 102 adds further weight against a serious examination burden. In addition, the previous rejection over a single reference under 35 U.S.C. § 102 appears to argue against the newly alleged multiple classifications.

As the history of examination fails to support the newly alleged multiple classifications, Applicants respectfully assert that the present six-way

restriction requirement is improper. For this further reason, Applicants respectfully solicit withdrawal of the restriction requirement.

In addition to the previous arguments in traverse of the restriction requirement, Applicants respectfully traverse at least the following classifications.

The Examiner alleges Group I, recited in claims 1-8 [sic], as classified in class 717, subclass 131. This class is defined as "data processing: software development, installation, and management, software program development tool [e.g., integrated case tool or stand-alone development tool], testing or debugging including analysis of program execution."

Applicants traverse this classification. Claim 1, allegedly part of Group I, recites:

> A method of executing a processor instruction, said method comprising:
>
> fetching from memory a first machine language instruction comprising an instruction segment;
>
> responsive to a trigger pattern in said first machine language instruction, modifying said instruction segment to form a second machine language instruction; and
>
> executing on said processor said second machine language instruction.

Applicants respectfully assert that the claimed limitations of Claim 1 are not directed to "software development," or "software program development tools," or "testing or debugging" or "analysis of program execution" as required by class 717, subclass 131.

For these reasons, Applicants respectfully assert that the classification of the alleged Group I invention is incorrect, and respectfully solicit correction of the classification. Moreover, as the classification of the alleged Group I invention is incorrect, Applicants respectfully assert that the basis for restriction is correspondingly incorrect. For this reason, Applicants respectfully solicit withdrawal of the restriction requirement.

The Examiner alleges Group III, recited in claims 17-22, as classified in class 712, subclass 25. This class is defined as "processing architecture: data driven or demand driven processor."

Applicants traverse this classification. Claim 17, allegedly part of Group III, recites:

A computer system comprising:

a memory for storing a first machine language instruction;

a processor coupled to said memory for executing machine language instructions;

said processor also for implementing a method, said method comprising: (the method recited in Claim 1).

Applicants respectfully assert that the claimed limitations of Claim 17 are not directed to a data driven or demand driven processor, as those terms are understood by those of ordinary skill in the art, and as they are used in the USPTO classification schedule for class 712, subclass 25.

For these reasons, Applicants respectfully assert that the classification of the alleged Group III invention is incorrect, and respectfully solicit correction of the classification. Moreover, as the classification of the alleged Group III invention is incorrect, Applicants respectfully assert that the basis for restriction is correspondingly incorrect. For this reason, Applicants respectfully solicit withdrawal of the restriction requirement.

Further with respect to alleged Group III, the alleged invention of Group III recites a processor for implementing the method recited in Claim 1 (Group I). Applicants fail to understand how a processor for implementing a method of a first group can attain status as an allegedly different group, under a separate classification.

For this further reason, Applicants respectfully solicit withdrawal of the restriction requirement.

The rejection argues that inventions I and III are separately usable, as invention I "which does not have the processor coupled to the memory for executing machine language instructions (as in Group III). Applicants respectfully traverse. Group I recites "executing on said processor said second machine language instruction." Thus, an apparatus for implementing the method of Group I must have a processor capable of executing machine language instructions, in contrast to the rejection's allegation. Further, Group III recites all the limitation of independent Claim 1 (Group I).

For this still further reason, Applicants respectfully solicit withdrawal of the restriction requirement.

The Examiner alleges Group IV, recited in claims 23-32, classified in class 717, subclass 143. This class is defined as "data processing: software development, installation, and management, compiling code, analysis of code form, parsing, syntax analysis, and semantic analysis."

Applicants traverse this classification. Claim 23, allegedly part of Group IV, recites:

a memory stored packet contained within a very long instruction word, said packet comprising

a trigger pattern to initiate modification of a segment of said very long instruction word;

a first field to indicate a portion of said segment to be modified; and

a second field to indicate how to modify said portion of said segment.

Applicants respectfully assert that the claimed limitations of Claim 23 are not directed to "software development," or "compiling code," or "analysis of code form" or "parsing" or "syntax analysis" or "semantic analysis" as required by class 717, subclass 143.

For these reasons, Applicants respectfully assert that the classification of the alleged Group IV invention is incorrect, and respectfully solicit correction of the classification. Moreover, as the classification of the alleged Group IV invention is incorrect, Applicants respectfully assert that the basis for restriction is correspondingly incorrect. For this reason, Applicants respectfully solicit withdrawal of the restriction requirement.

35 U.S.C. § 102

Claims 1-5 stand rejected under 35 U.S.C. § 102(b) as being allegedly anticipated by Nunomura (US 6,871,274, "Nunomura"). Applicants have carefully reviewed the cited reference and respectfully assert that embodiments of the present invention as recited in Claims 1-5 are patentable over Nunomura.

With respect to Claim 1, Applicants respectfully assert that Nunomura fails to teach or suggest the limitation of "fetching a first machine language instruction" as recited by Claim 1. Applicants respectfully assert that the rejection improperly equates the taught "compressed instruction code" with the recited machine language instruction.

In contrast, Nunomura teaches "a compressed instruction code" (column 2, lines 2-3, *inter alia*). In addition, Nunomura teaches that such "compressed instruction code" is accessed by "an instruction code conversion apparatus" (column 2, lines 1-2, *inter alia*) and not by an "instruction decode unit" (column 5 lines 6-20), as are other machine language instructions.

Thus, Nunomura teaches that the relied upon teaching is not "a machine language instruction" as claimed by Claim 1. Nunomura's "compressed instruction code" is not recognized as an instruction code, and must be converted into an instruction code, in much the same manner that a digitally

compressed music, e.g., an MP3, is not sound, and must be converted into a different data structure before it can be played.

Further, Nunomura teaches, "an instruction code conversion apparatus converts a first code to a second code longer in bit length than the first code to create an instruction code" (column 2, lines 17-19, *inter alia*). In teaching that an "instruction code" is created, Nunomura teaches that the taught "first code," also known as a "compressed instruction code," is not an "instruction code." Consequently, Applicants respectfully assert that Nunomura teaches that the "compressed instruction code" is not a machine language instruction. Applicants respectfully further assert that one of ordinary skill in the art would not understand the taught "compressed instruction code" to teach or suggest the recited "machine language instruction" as recited by Claim 1.

Still further, Nunomura teaches that the "compressed instruction code" is "unrecognizable as an instruction code" (column 7 lines 30-37).

Applicants assert that an element that is "unrecognizable as an instruction code," as taught by Nunomura, is not, and cannot be an "instruction code." Nunomura teaches that it is not. Thus, the cited reference itself directly contradicts the rejection's allegation.

For these reasons, Applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

In addition with respect to Claim 1, Applicants respectfully assert that Nunomura fails to teach or suggest the limitation of "modifying said instruction segment to form a second machine language instruction" as recited by Claim 1.

Claim 1 recites that the instruction segment is part of a first machine language instruction. The cited reference itself teaches that that the accessed data structure is not a machine language instruction. Thus, no segment of a non-machine language instruction can be part of a machine language instruction. Even if, *arguendo*, the taught "compressed instruction code" suggests a machine language instruction, Nunomura fails to teach or suggest the limitation of "modifying said instruction segment" as recited by Claim 1.

As taught by Nunomura, a segment of the "compressed instruction code" is replaced by a second code "longer in bit length than the first code" (column 2 lines 18-19). For example, Figure 4 shows a four-bit "index" mapping into a 24 bit op code. Applicants respectfully assert that a code segment "longer in bit length than the first code" as taught by Nunomura, cannot be the recited "instruction segment" that is part of the recited first machine language instruction. Applicants respectfully assert that an "instruction segment" as

recited by Claim 1 cannot simultaneously be both four bits and 24 bits long. Further, Applicants respectfully assert that an alleged first machine language instruction taught as 16 bits in length cannot comprise an "instruction segment" of 24 bits in length.

Further, the alleged 24-bit instruction segment will not fit in the 12 or 16-bit machine language instructions taught by Nunomura. Thus, the 24-bit field cannot be a segment of a 12 or 16 bit machine language instruction.

For this additional reason, Applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Applicants respectfully assert that Claims 2-7 overcome the rejections of record by virtue of their dependency, and respectfully solicit allowance of these Claims.

In addition with respect to Claim 2, Applicants respectfully assert that Nunomura fails to teach or suggest the limitation of "substitut(ing) a bit pattern of a subset of said instruction segment" as recited by Claim 2. In contrast, Nunomura teaches "substituting" more bits than an instruction segment contains. In this manner, Nunomura actually teaches away from the recited

limitation of substituting a subset of bits of an instruction segment, as recited by Claim 2.

For this additional reason, Applicants respectfully assert that Claim 2 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

In addition with respect to Claim 4, Applicants respectfully assert that Nunomura fails to teach or suggest the limitation of "executing microcode" as recited by Claim 4. Applicants respectfully assert that Nunomura is silent as to such recited microcode. Applicants respectfully note that Figure 4, cited in rejecting Claim 4, refers to compressed instructions and instruction codes. Such codes do not teach or suggest microcode, as used by those of skill in the art, as explained in the present application and as recited in the instant claim.

For this additional reason, Applicants respectfully assert that Claim 4 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Claims 1-7 stand rejected under 35 U.S.C. § 102(b) as being allegedly anticipated by Tremblay et al. (US 5,925,123, "Tremblay"). Applicants have

carefully reviewed the cited reference and respectfully assert that embodiments of the present invention as recited in Claims 1-7 are patentable over Tremblay.

With respect to Claim 1, Applicants respectfully assert that Tremblay fails to teach or suggest the limitation of "responsive to a trigger pattern in said first machine language instruction, modifying said instruction segment to form a second machine language instruction" as recited by Claim 1.

In contrast, Tremblay teaches that a specific Java bytecode 701switches the mode of the processor, e.g., to a RISC execution unit (column 27, lines 40-53). While this portion of an instruction may modify an operating mode of a processor, it fails to modify any portion of the instruction, e.g., other instruction 702 (Figure 7). Further, Tremblay is absolutely and completely silent as to forming a "second machine language instruction" from a first machine language instruction" as recited by Claim 1.

Moreover, Tremblay teaches "[c]onsequently, instruction decoder 135, or other hardware in processor 600 routes information 702 to second instruction decoder 660..." (column 27, lines 53-58). Tremblay further teaches, "upon execution of a predefined instruction in the datastream, the datastream is toggled to a second instruction decoder 660 that is activated to process

subsequent information in the datastream" (column 28 lines 8-12, emphasis added).

Thus, Tremblay teaches that unmodified information in the datastream is executed without modification, in direct opposition to the claimed limitation of modifying an instruction segment to form a new instruction. Tremblay does not modify, and hence does not teach or suggest at least this claimed element.

For this reason, Applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Applicants respectfully assert that Claims 2-7 overcome the rejections of record by virtue of their dependency, and respectfully solicit allowance of these Claims.

In addition with respect to Claim 2, Applicants respectfully assert that Tremblay fails to teach or suggest the claimed limitation "wherein said modifying substitutes a bit pattern of a subset of said instruction segment" as recited by Claim 2. As previously presented with respect to Claim 1, Tremblay does not modify, and hence does not teach or suggest at least this claimed element.

For this additional reason, Applicants respectfully assert that Claim 2 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

35 U.S.C. § 103

Claims 6 and 7 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Nunomura (US 6,871,274, "Nunomura") in view of Rim (US 6,202,143, "Rim"). Applicants have carefully reviewed the cited references and respectfully assert that embodiments of the present invention as recited in Claims 6 and 7 are patentable over Nunomura in view of Rim.

With respect to Claims 6 and 7, Applicants respectfully assert that the proposed manner of combination of Nunomura in view of Rim is not supported by the references. Rim teaches multiple program memories for storing multiple sizes of instruction words, and that the multiple program memories "preferably have different (bus) widths" (Abstract). In contrast, Nunomura teaches a single memory with a single bus size. Applicants respectfully assert that one of ordinary skill in the art would not be motivated to combine these references in the manner suggested because of the complexity of Rim in contrast to the relative simplicity of Nunomura.

Applicants respectfully assert that one of ordinary skill in the art would understand a simpler system to be preferable to a more complex system, for accomplishing the same result. For example, "increased complexity" is not an advantage, and therefore provides no rationale for combining references, particularly in the manner proposed by the rejection.

For this reason, Applicants respectfully assert that the proposed combination of Nunomura in view of Rim does not motivate the claimed subject matter, and that all rejections dependent upon this combination of references are overcome. The rejection proposes, as motivation for the proposed manner of combination, that one of ordinary skill would be motivated to increase the adaptability of Nunomura to accept long instruction words. Applicants respectfully traverse. There is no teaching in the prior art as to the desirability of modifying Nunomura to accept VLIW instructions. Moreover, Nunomura fails to teach or suggest the multiple instruction units necessary to process a VLIW instruction. Thus, even if Nunomura was modified in view of Rim to "recognize() ... specific instruction type with corresponding width of the Rim's VLIW," the proposed combination would be unable to execute such VLIW instructions. Applicants respectfully assert that one of ordinary skill in the art would not be motivated to modify Nunomura in view of Rim, in the manner proposed by the rejection, to "recognize" VLIW instructions in spite of a lack of capability to execute such instructions.

For this additional reason, Applicants respectfully assert that the proposed manner of combination of Nunomura in view of Rim is not suggested by the cited references, and that all rejections dependent upon this combination of references are overcome. Applicants respectfully solicit allowance of Claims 6 and 7.

Further, Nunomura teaches a method of storing instructions in a compressed format. In contrast, Rim teaches a method of expanding a complete uncompressed instruction with meaningless filler (a "NOP" or no operation instruction) to fill a wide bus. Applicants respectfully assert that, in consideration of the whole of the teachings of Nunomura and Rim, one of ordinary skill in the art would not be motivated to modify a decompression process with a process that places meaningless filler into an instruction word. Moreover, Nunomura has no need for the filler methods of Rim, as Nunomura has a single bus and a single bus width.

For this further reason, Applicants respectfully assert that the proposed combination of Nunomura in view of Rim is improper, and that all rejections dependent upon this combination of references are overcome. Applicants respectfully solicit allowance of Claims 6 and 7.

With respect to Claims 6 and 7, Applicants respectfully assert that Nunomura fails to teach or suggest the limitation of "fetching a first machine language instruction" as recited by the instant Claims, for at least the rationale previously presented with respect to Claim 1. As Rim fails to correct this deficiency of Nunomura, Applicants respectfully assert that Claims 6 and 7 overcome the rejections of record, and respectfully solicit allowance of these Claims.

Applicants respectfully assert that Claims 6 and 7 overcome the rejections of record by virtue of their dependency, and respectfully solicit allowance of these Claims.

In addition with respect to Claim 6, Applicants respectfully assert that Nunomura in view of Rim fails to teach or suggest the limitation of "wherein said first machine language instruction comprises a very long instruction word" as recited by Claim 6. Applicants are unclear as to what format a compressed instruction code might have under the modification proposed by the rejection, but respectfully assert that such a compressed instruction code would not be a very long instruction word as specifically recited by Claim 6.

While Nunomura in view of Rim may allegedly teach some form of manipulating a first bit pattern to produce a second bit pattern, wherein the

second bit pattern is a VLIW instruction, the recited limitation refers to accessing a VLIW instruction, e.g., the allegedly taught first bit pattern must be a VLIW instruction. Applicants understand that it is the intention of Nunomura is to reduce the size of such compressed instruction codes. Hence, Nunomura leads away from the recited fetching VLIW machine language instructions as recited by Claim 6.

For this additional reason, Applicants respectfully assert that Claim 6 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

CONCLUSION

Claims 1-45 are pending in the present application. Applicants respectfully request reconsideration of the present application in view of the amendments and remarks presented herein.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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